APPARATUS AND METHOD FOR COMPRESSION OF THE TIMING TRACE STREAM

This application claims priority under 35 USC §119(e)(1) of Provisional Application Number 60/434,176 (TI-34670P) filed December 17, 2002.

Related Applications

U.S. Patent Application (Attorney Docket No. TI-34654), entitled APPARATUS AND METHOD FOR SYNCHRONIZATION OF TRACE STREAMS FROM MULTIPLE PROCESSORS, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34655), entitled APPARATUS AND METHOD FOR SEPARATING DETECTION AND ASSERTION OF A TRIGGER EVENT, invented by Gary L. Swoboda, filed on

even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI- 34656), entitled APPARATUS AND METHOD FOR STATE SELECTABLE TRACE STREAM GENERATION, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34657), entitled APPARATUS AND METHOD FOR SELECTING PROGRAM HALTS IN AN UNPROTECTED PIPELINE AT NON-INTERRUPTIBLE POINTS IN CODE EXECUTION, invented by Gary L. Swoboda and Krishna Allam, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34658), entitled APPARATUS AND METHOD FOR REPORTING PROGRAM HALTS IN AN UNPROTECTED PIPELINE AT NON-INTERRUPTIBLE POINTS IN CODE EXECUTION, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34659), entitled APPARATUS AND METHOD FOR A FLUSH PROCEDURE IN AN INTERRUPTED TRACE STREAM, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34660), entitled APPARATUS AND METHOD FOR CAPTURING AN EVENT OR COMBINATION OF EVENTS RESULTING IN A TRIGGER SIGNAL IN A TARGET PROCESSOR, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application;

U.S. Patent Application (Attorney Docket No. TI-34661), entitled APPARATUS AND METHOD FOR CAPTURING THE PROGRAM COUNTER ADDRESS ASSOCIATED WITH A TRIGGER SIGNAL IN A TARGET PROCESSOR, invented by Gary L. Swoboda, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34662), entitled APPARATUS AND METHOD DETECTING ADDRESS CHARACTERISTICS FOR USE WITH A TRIGGER GENERATION UNIT IN A TARGET PROCESSOR, invented by Gary Swoboda and Jason L. Peck, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34663), entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PROCESSOR RESET, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent (Attorney Docket No. TI-34664), entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PROCESSOR DEBUG HALT SIGNAL, invented by Gary L. Swoboda, Bryan Thome, Lewis Nardini and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34665), entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PIPELINE FLATTENER PRIMARY CODE FLUSH FOLLOWING INITIATION OF AN INTERRUPT SERVICE ROUTINE; invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the

assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34666), entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PIPELINE FLATTENER SECONDARY CODE FLUSH FOLLOWING A RETURN TO PRIMARY CODE EXECUTION, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Docket No. TI-34667), entitled APPARATUS AND METHOD IDENTIFICATION OF A PRIMARY CODE START SYNC POINT FOLLOWING A RETURN TO PRIMARY CODE EXECUTION, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U. S. Patent Application (Attorney Docket No. TI-34668), entitled APPARATUS AND METHOD FOR IDENTIFICATION OF A NEW SECONDARY CODE START POINT FOLLOWING A RETURN FROM A SECONDARY CODE EXECUTION, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34669), entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PAUSE POINT IN A CODE EXECTION SEQUENCE, invented by Gary L. Swoboda, Bryan Thome and Manisha Agarwala, filed on even date herewith, and assigned to the assignee of the present application; U.S. Patent Application (Attorney Docket No. TI-34671), entitled APPARATUS AND METHOD FOR TRACE STREAM IDENTIFCATION OF MULTIPLE TARGET PROCESSOR EVENTS, invented

by Gary L. Swoboda and Bryan Thome, filed on even date herewith, and assigned to the assignee of the present application; and U.S. Patent Application (Attorney Docket No. TI-34672 entitled APPARATUS AND METHOD FOR OP CODE EXTENSION IN PACKET GROUPS TRANSMITTED IN TRACE STREAMS, invented by Gary L. Swoboda and Bryan Thome, filed on even date herewith, and assigned to the assignee of the present application are related applications.

Background of the Invention

1. Field of the Invention

This invention relates generally to the testing of digital signal processing units and, more particularly, to the signals that are transmitted from a target processor to a host processing unit to permit analysis of the target processor operation. Certain events in the target processor must be communicated to the host processing unit along with contextual information. In this manner, the test and debug data can be analyzed and problems in the operation of the target processor identified.

2. Description of the Related Art

As microprocessors and digital signal processors have become increasingly complex, advanced techniques have been

developed to test these devices. Dedicated apparatus is available to implement the advanced techniques. Referring to Fig. 1, a general configuration for the test and debug of a target processor **12** is shown. The test and debug procedures operate under control of a host processing unit **10**. The host processing unit **10** applies control signals to the emulation unit **11** and receives (test) data signals from the emulation unit **11** by cable connector **14**. The emulation unit **11** applies control signals to and receives (test) signals from the target processing unit **12** by connector cable **15**. The emulation unit **11** can be thought of as an interface unit between the host processing unit **10** and the target processor **12**. The emulation unit **11** processes the control signals from the host processor unit **10** and applies these signals to the target processor **12** in such a manner that the target processor will respond with the appropriate test signals. The test signals from the target processor **12** can be a variety types. Two of the most popular test signal types are the JTAG (Joint Test Action Group) signals and trace signals. The JTAG protocol provides a standardized test procedure in wide use in which the status of selected components is determined in response to control signals from the host processing unit. Trace signals are signals from a multiplicity of selected locations in the target processor **12** during defined period of operation. While the width of the bus **15** interfacing to the host processing unit **10** generally has a standardized dimension,

the bus between the emulation unit **11** and the target processor **12** can be increased to accommodate an increasing amount of data needed to verify the operation of the target processing unit **12**. Part of the interface function between the host processing unit **10** and the target processor **12** is to store the test signals until the signals can be transmitted to the host processing unit **10**.

In the prior art, the trace streams carry test and debug data from the target processor to the host processing unit in signal groups, the signal groups including signal packets. The trace packets are groups of data, a plurality of packets typically being transmitted together. The packets can be relatively small, e.g., each packet has an 8 bit payload (information signal group) in the preferred embodiment. The small size of the packets permits great flexibility in transmission through non-standardized interfaces. One of the trace streams is typically a timing trace stream. Each timing packet group typically includes a header packet and a plurality of information packets. The timing data identifies an activity or a non-activity of the program counter during each clock cycle. Therefore, a logic signal must be transmitted for each clock cycle of the target processing unit in order to reconstruct the activity of the target processor. Moreover, an appreciable part of the bandwidth of the trace streams can be used in transmission of the timing data. Because of the large

amount of data that must be transmitted from the increasingly complex target processors to host processing unit for analysis, minimizing the transmission of data is important.

A need has been felt for apparatus and an associated method having the feature of reducing the amount of information that must be transmitted by the trace stream to the host processing unit. It would be another feature of the apparatus and associated method to reduce the amount of information used to represent the timing parameters of target processing unit. It would be yet another feature of the apparatus and associated method to provide flexibility in transmitting data in timing packet groups. It would a still another feature of the apparatus and associated method to provide timing packet groups capable of compressing the timing information of the target processor. It is a more particular feature of the apparatus and associated method to replace a timing packet group in which each data bit position represents the same logic signal with a smaller timing packet group.

Summary of the Invention

The aforementioned and other features are accomplished, according to the present invention, by providing timing trace generation unit that has a first storage unit wherein a sequence of logic signals relating to the activity of the program counter associated with each clock cycle is formed into packet groups. The contents of the first storage unit are typically transferred to the host processing unit for analysis. A second storage unit includes a count of the number of bit positions for storing the logic signals of the first storage unit. A logic unit determines when all of the signals in the first storage unit have the same logic value. When this determination is made, an indicia of the same logic value is stored in a header portion of the second storage unit and the contents of the second storage unit are transmitted to the host processing unit in place of the contents of the first storage unit. Because the second storage unit is smaller than the first storage unit, a saving in the amount of transmitted information is achieved.

Other features and advantages of present invention will be more clearly understood upon reading of the following description and the accompanying drawings and the claims.

Brief Description of the Drawings

Figure 1 is a general block diagram of a system configuration for test and debug of a target processor according to the prior art.

Figure 2 is a block diagram of selected components in the target processor used the testing of the central processing unit of the target processor according to the present invention.

Figure 3 is a block diagram of selected components of the illustrating the relationship between the components transmitting trace streams in the target processor.

Figure 4A illustrates format by which the timing packets are assembled according to the present invention; while Figure 4B illustrates how the packets in the timing trace stream are formed from the timing signals.

Figure 5A illustrates a packet group in a typical timing trace stream, while Figure 5B illustrates a compressed packet group according to the present invention.

Figure 6 is a block diagram for generating either a typical group of packets or a compressed group of packets according to the present invention.

Description of the Preferred Embodiment

1. Detailed Description of the Figures

Fig. 1A and Fig. 1B have been described with respect to the related art.

Referring to Fig. 2, a block diagram of selected components of a target processor **20**, according to the present invention, is shown. The target processor includes at least one central processing unit **200** and a memory unit **208**. The central processing unit **200** and the memory unit **208** are the components being tested. The trace system for testing the central processing unit **200** and the memory unit **202** includes three packet generating units, a data packet generation unit **201**, a program counter packet generation unit **202** and a timing packet generation unit **203**. The data packet generation unit **201** receives VALID signals, READ/WRITE signals and DATA signals from the central processing unit **200**. After placing the signals in packets, the packets are applied to the scheduler/multiplexer unit **204** and forwarded to the test and debug port **205** for transfer to the emulation unit **11**. The program counter packet generation unit **202** receives PROGRAM COUNTER signals, VALID signals, BRANCH signals, and BRANCH TYPE signals from the central processing unit **200** and, after

forming these signal into packets, applies the resulting program counter packets to the scheduler/multiplexer **204** for transfer to the test and debug port **205**. The timing packet generation unit **203** receives ADVANCE signals, VALID signals and CLOCK signals from the central processing unit **200** and, after forming these signal into packets, applies the resulting packets to the scheduler/multiplexer unit **204** and the scheduler/multiplexer **204** applies the packets to the test and debug port **205**. Trigger unit **209** receives EVENT signals from the central processing unit **200** and signals that are applied to the data trace generation unit **201**, the program counter trace generation unit 202, and the timing trace generation unit **203**. The trigger unit **209** applies TRIGGER and CONTROL signals to the central processing unit **200** and applies CONTROL (i.e., STOP and START) signals to the data trace generation unit **201**, the program counter generation unit **202**, and the timing trace generation unit **203**. The sync ID generation unit **207** applies signals to the data trace generation unit **201**, the program counter trace generation unit **202** and the timing trace generation unit **203**. While the test and debug apparatus components are shown as being separate from the central processing unit **201**, it will be clear that an implementation these components can be integrated with the components of the central processing unit **201**.

Referring to Fig. 3, the relationship between selected components in the target processor **20** is illustrated. The data trace generation unit **201** includes a packet assembly unit **2011** and a FIFO (first in/first out) storage unit **2012**, the program counter trace generation unit **202** includes a packet assembly unit **2021** and a FIFO storage unit **2022**, and the timing trace generation unit **203** includes a packet generation unit **2031** and a FIFO storage unit **2032**. As the signals are applied to the packet generators **201**, **202**, and **203**, the signals are assembled into packets of information. The packets in the preferred embodiment are 10 bits in width. Packets are assembled in the packet assembly units in response to input signals and transferred to the associated FIFO unit. The scheduler/multiplexer **204** generates a signal to a selected trace generation unit and the contents of the associated FIFO storage unit are transferred to the scheduler/multiplexer **204** for transfer to the emulation unit. Also illustrated in Fig. 3 is the sync ID generation unit **207**. The sync ID generation unit **207** applies an SYNC ID signal to the packet assembly unit of each trace generation unit. The periodic signal, a counter signal in the preferred embodiment, is included in a current packet and transferred to the associated FIFO unit. The packet resulting from the SYNC ID signal in each trace is transferred to the emulation unit and then to the host processing unit. In the host processing unit, the same

count in each trace stream indicates that the point at which the trace streams are synchronized. In addition, the packet assembly unit **2031** of the timing trace generation unit **203** applies and INDEX signal to the packet assembly unit **2021** of the program counter trace generation unit **202**. The function of the INDEX signal will be described below.

Referring to Fig. 4A, the assembly of timing packets is illustrated. The signals applied to the timing trace generation unit **203** are the CLOCK signals and the ADVANCE signals. The CLOCK signals are system clock signals to which the operation of the central processing unit **200** is synchronized. The ADVANCE signals indicate an activity such as a pipeline advance or program counter advance (()) or a pipeline non-advance or program counter non-advance (1). An ADVANCE or NON-ADVANCE signal occurs each clock cycle. The timing packet is assembled so that the logic signal indicating ADVANCE or NON-ADVANCE is transmitted at the position of the concurrent CLOCK signal. These combined CLOCK/ADVANCE signals are divided into groups of 8 signals, assembled with two control bits in the packet assembly unit **2031**, and transferred to the FIFO storage unit **2032**.

Referring to Fig. 4B, the trace stream generated by the timing trace generation unit **203** is illustrated. The first (in time) trace packet is generated as before. During the

assembly of the second trace packet, a SYNC ID signal is generated during the third clock cycle. In response, the timing packet assembly unit **2031** assembles a packet in response to the SYNC ID signal that includes the sync ID number. The next timing packet is only partially assembled at the time of the SYNC ID signal. In fact, the SYNC ID signal occurs during the third clock cycle of the formation of this timing packet. The timing packet assembly unit **2031** generates a TIMING INDEX 3 signal (for the third packet clock cycle at which the SYNC ID signal occurs) and transmits this TIMING INDEX 3 signal to the program counter packet assembly unit **2031**.

Referring to Fig, 5A, a typical packet group **50** in the timing stream is illustrated. The packet group consists of four packets **502**, each packet **502** having an 8 bit payload. In the preferred embodiment, an addressable memory location in the host processing unit stores 32 bits. The 2 bit control signals indicated that what is being transmitted in the timing trace stream is a series of 8 bit payload packets. As indicated above, the timing trace stream includes periodic sync markers that can synchronize the plurality of trace streams.

Referring to Fig. 5B, compressed packet group **55**, according to the present invention, is shown. In this packet group **55**, a 10 bit packet is transmitted. However, the control

signals are selected to indicate that a different interpretation of the payload is required. In particular, the payload is an indication of the number of 32 bit timing packets, coincident with the memory location boundaries that transmit the same logic signal. If, for example, the packet group **50** included logic signals having the same value, then the packet group **50** is replaced by a packet **55**. Several consecutive packets groups **50**, in which the payload of each packet **502** has the same logic value, can be replaced by the packet **55**. The packet **55** identifies the number of packet groups **50** having the same logic signal group in the packet payloads. In this manner, the timing trace stream can be compressed.

Referring to Fig. 6, a block diagram of the timing stream generation unit **203** capable of performing the compression of the timing trace stream is shown. The packet assembly unit **2031** includes two storage units **20311** and **20312**, a logic unit **20314**, and a switch **20313**. The timing sequence signals, a logic "1" or a logic "0" during each clock cycle is applied to storage unit **20311**, to logic unit **30314**, and to storage unit **20312**. The timing sequence signals applied to storage unit **20311** fill the 32 bit (payload) positions in packet group **50**. At the same time, the timing sequence signals are applied to the logic bit position **551A** of the header packet **551** of the compressed packet group. In addition, the timing sequence signals are applied to the

logic unit **20314**. When the first bit position is filled in the storage unit, the logic unit begins to count the applied logic signals. When the first signal is entered in the storage unit **20311**, the first count has been made in logic unit **20314**. When the count in logic unit **20314** reaches 32, a control signal is applied to switch **20313**. When all the logic signals of the timing sequence have the same value, a first control signal applied to the switch results in the contents of storage unit **20312** (i.e., packet group **55**) being applied to the FIFO unit **2032**. Because the timing sequence signals are applied to the header location **551A** in storage unit **20312**, when the packet group from storage unit **20312** is transferred to the FIFO unit, the logic signal in location **551A** is the logic signal to which the 32 count of packet **55** refers. When the logic signals applied to logic unit **20314** have different logic states during the 32 clock cycles during which the storage unit **20311** is filled, a second logic signal from the logic unit **20314** applied to switch **20313** results in the contents of storage unit **20311** (i.e., packet group **50**) being applied to the FIFO unit **2032**.

2. Operation of the Preferred Embodiment

The present invention is directed toward minimizing the amount of data transferred from the target processor to the host processing unit while accurately reflecting the

operation of the target processor. The present invention provides for the compression of the timing trace stream. This compression of the timing trace stream is the result of the recognition that many situations occur when a lengthy sequence of all logic "1"s or of all logic "0"s can occur. When the sequence of the same logic signals coincides with the a normal timing stream packet group as determined by the filling of the storage locations of the first storage unit in Fig. 6, a small packet group can be used to replace the typical normal timing stream trace group. The normal timing trace stream packet group has a predetermined payload (i.e., standard count of clock cycles) in each multi-packet group. This payload is selected to expedite storage of the logic signals in storage unit of the host processing unit.

As indicated in Fig. 5B, the standard count is included in information packet. A second packet is needed because it may be expedite for testing different target devices to be capable of programming signal group in the information packet. In addition, the logic unit may be chosen to identify one than one standard count of clock cycle. In this embodiment, the logic device can identify the number of standard count of clock cycles and enter this number in information packet. In this embodiment, the compressed timing packet group is transferred to the FIFO unit when,

after the first standard count of clock cycles is completed, a different logic value is identified.

When the standard count of clock cycles is non-changing, then the transmission of the header packet alone can provide the information concerning the single logic signal during the standard count of clock cycles. When the logic signal does not change for more than one standard count of clock cycles, then the number of standard clock cycles can be included in the information packet or in the header packet of the compressed timing group.

While the present timing trace stream has used the control signals to describe the function of the associated packet, the used o packets groups with header could also be used to interpret the payload of the packet. The present invention provides a technique for compressing this timing trace stream format.

While the invention has been described with respect to the embodiments set forth above, the invention is not necessarily limited to these embodiments. Accordingly, other embodiments, variations, and improvements not described herein are not necessarily excluded from the scope of the invention, the scope of the invention being defined by the following claims.